1. A regulator circuit for a voltage pump, said regulator circuit comprising:

voltage divider means connected between a first and second voltage, said voltage divider means generating a reference voltage;

first adjustment means for adjusting a resistance of said voltage divider means to modify a voltage level of the reference voltage;

second adjustment means for adjusting the resistance of said voltage divider means to modify the voltage level of the reference voltage;

first connection means for connecting said first adjustment means to said voltage divider means in response to a first control signal, said first connection means disconnecting said first adjustment means from said voltage divider means when the first control signal is not received; and

second connection means for connecting said second adjustment means to said voltage divider means in response to a second control signal, said second connection means disconnecting said second adjustment means from said voltage divider means when the second control signal is not received, wherein said first and second control signals independently control said first and second connection means.

2. The circuit of claim 1, wherein the first control signal is generated based on an operating mode of the circuit.

3. The circuit of claim 2, wherein the first control signal is generated when the operating mode is a nominal operating mode.

4. The circuit of claim 2, wherein the first control signal is generated when the operating mode is a burn-in operating mode.

5. The circuit of claim 2, wherein the first control signal is generated when the operating mode is a power-up operating mode.

6. The circuit of claim 1, wherein the second control signal is generated based on an operating mode of the circuit.

7. The circuit of claim 6, wherein the second control signal is generated when the operating mode is a nominal operating mode.

8. The circuit of claim 6, wherein the second control signal is generated when the operating mode is a burn-in operating mode.

9. The circuit of claim 6, wherein the second control signal is generated when the operating mode is a power-up operating mode.

10. The circuit of claim 1, wherein said voltage divider means comprises a series of resistance elements and said first adjustment means comprises a series of switching elements that are connected across respective resistance elements in response to the first control signal.

11. The circuit of claim 10, wherein each switching element can be independently placed into an active state, which switches out its respective resistance element.

12. The circuit of claim 10, wherein each switching element can be independently placed into an inactive state, which switched in its respective resistance element.

13. The circuit of claim 1, wherein said voltage divider circuit comprises a series of resistance elements and said second adjustment means comprises a series of switching elements that are connected across respective resistance elements in response to the second control signal.

14. The circuit of claim 13, wherein each switching element can be independently placed into an active state, which switches out its respective resistance element.

15. The circuit of claim 13, wherein each switching element can be independently placed into an inactive state, which switches in its respective resistance element.

16. The circuit of claim 1 further comprising level detecting means, said level detecting means receiving the reference voltage and generating a signal to operate the voltage pump.

17. A regulator circuit for a voltage pump, said regulator circuit comprising:

a voltage divider circuit connected between a first and second voltage, said voltage divider circuit having a resistance and outputting a reference voltage;

a first adjustment circuit;

a first connection circuit, said first connection circuit connecting said first adjustment circuit to said voltage divider circuit in response to a first control signal and disconnecting said first adjustment circuit from said voltage divider circuit when the first control signal is not received, said first adjustment circuit when connected to said voltage divider circuit adjusting the resistance of said voltage divider circuit to modify a voltage level of the reference voltage;

a second adjustment circuit; and

a said connection circuit, said second connection circuit connecting said second adjustment circuit to said voltage divider circuit in response to a second control signal and disconnecting said second adjustment circuit from said voltage divider circuit when the second control signal is not received, said second adjustment circuit when connected to said voltage divider circuit adjusting the resistance of said voltage divider circuit to modify a voltage level of the reference voltage, wherein said first and second control signals independently control said first and second connection circuit based upon an operating mode of said regulator circuit.

18. A regulator circuit for a voltage pump comprising:

a voltage divider having a resistance, said voltage divider generating a reference voltage based on the resistance; and

at least two independently selectable and adjustable adjustment circuits connected to said voltage divider, each adjustment circuit being selectable by a respective control signal and being adjustable to adjust the resistance of said

voltage divider such that the reference voltage is generated at a predetermined level for a particular operating mode.

19. A memory circuit comprising:

a memory array;

a voltage pump for supplying pump voltage to said memory array; and

a regulator circuit connected to said voltage pump, said regulator circuit comprising:

a voltage divider circuit connected between a first and second voltage, said voltage divider circuit having a resistance and outputting a reference voltage used to operate said pump;

a first adjustment circuit;

a first connection circuit, said first connection circuit connecting said first adjustment circuit to said voltage divider circuit in response to a first control signal and disconnecting said first adjustment circuit from said voltage divider circuit when the first control signal is not received, said first adjustment circuit when connected to said voltage divider circuit adjusting the resistance of said voltage divider circuit to modify a voltage level of the reference voltage;

a second adjustment circuit; and

a said connection circuit, said second connection circuit connecting said second adjustment circuit to said voltage divider circuit in response to a second

control signal and disconnecting said second adjustment circuit from said voltage divider circuit when the second control signal is not received, said second adjustment circuit when connected to said voltage divider circuit adjusting the resistance of said voltage divider circuit to modify a voltage level of the reference voltage, wherein said first and second control signals independently control said first and second connection circuit based upon an operating mode of said regulator circuit.

20. The circuit of claim 19, wherein the first control signal is generated when the operating mode is a nominal operating mode.

21. The circuit of claim 19, wherein the first control signal is generated when the operating mode is a burn-in operating mode.

22. The circuit of claim 19, wherein the first control signal is generated when the operating mode is a power-up operating mode.

23. The circuit of claim 19, wherein the second control signal is generated when the operating mode is a nominal operating mode.

24. The circuit of claim 19, wherein the second control signal is generated when the operating mode is a burn-in operating mode.

25. The circuit of claim 19, wherein the second control signal is generated when the operating mode is a power-up operating mode.

26. The circuit of claim 19, wherein the voltage divider circuit comprises a series of resistance elements and said first adjustment circuit comprises a series of

shunting elements that are connected across respective resistance elements in response to the first control signal.

27. The circuit of claim 26, wherein each shunting element can be independently placed into an active state, which shunts its respective resistance element.

28. The circuit of claim 27, wherein each shunting element can be independently placed into an inactive state, which does not shunt its respective resistance element.

29. The circuit of claim 19, wherein said voltage divider circuit comprises a series of resistance elements and said second adjustment circuit comprises a series of shunting devices that are connected across respective resistance elements in response to the second control signal.

30. The circuit of claim 29, wherein each shunting device can be independently placed into an active state, which shunts its respective resistance element.

31. The circuit of claim 30, wherein each shunting device can be independently placed into an inactive state, which does not shunt in its respective resistance element.

32. The circuit of claim 19 further comprising a level detect circuit that receives the reference voltage and generates a signal to operate said voltage pump.

33. A memory circuit comprising:

a memory array;

a voltage pump for supplying a pump voltage to said memory array; and

a regulator circuit connected to said voltage pump, said regulator circuit comprising:

a voltage divider having a resistance, said voltage divider generating a reference voltage based on the resistance, said reference voltage being used to operate said pump; and

at least two independently selectable and adjustable adjustment circuits connected to said voltage divider, each adjustment circuit being selectable by a respective control signal and being adjustable to adjust the resistance of said voltage divider such that the reference voltage is generated at a predetermined level for a particular operating mode.

34. A processor system comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit including a memory array, voltage pump for supplying a pump voltage to said array, and a regulator circuit connected to said voltage pump, said regulator circuit comprising:

a voltage divider circuit connected between a first and second voltage, said voltage divider circuit having a resistance and outputting a reference voltage used to operate said pump;

a first adjustment circuit;

a first connection circuit, said first connection circuit connecting said first adjustment circuit to said voltage divider circuit in response to a first control signal and disconnecting said first adjustment circuit from said voltage divider circuit when the first control signal is not received, said first adjustment circuit when connected to said voltage divider circuit adjusting the resistance of said voltage divider circuit to modify a voltage level of said reference voltage;

a second adjustment circuit; and

a said connection circuit, said second connection circuit connecting said second adjustment circuit to said voltage divider circuit in response to a second control signal and disconnecting said second adjustment circuit from said voltage divider circuit when the second control signal is not received, said second adjustment circuit when connected to said voltage divider circuit adjusting the resistance of said voltage divider circuit to modify a voltage level of said reference voltage, wherein said first and second control signals independently control said first and second connection circuit based upon an operating mode of said regulator circuit.

35. A processor system comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit including a memory array, voltage pump for providing a pumped voltage to said array, and a regulator circuit connected to said voltage pump, said regulator circuit comprising:

voltage divider means connected between a first and second voltage, said voltage divider means generating a reference voltage for operating said pump;

first adjustment means for adjusting a resistance of said voltage divider means to modify a voltage level of said reference voltage;

second adjustment means for adjusting the resistance of said voltage divider means to modify the voltage level of said reference voltage;

first connection means for connecting said first adjustment means to said voltage divider means in response to a first control signal, said first connection means disconnecting said first adjustment means from said voltage divider means when the first control signal is not received; and

second connection means for connecting said second adjustment means to said voltage divider means in response to a second control signal, said second connection means disconnecting said second adjustment means from said voltage divider means when the second control signal is not received, wherein said first and second control signals independently control said first and second connection means.